




NATIONAL INSTITUTE OF TECHNOLOGY, ARUNACHAL PRADESH

(Established by Ministry of Human Resources Development, Govt. Of India)

Yupia, District Papum Pare, Arunachal Pradesh - 791112

Fax: 0360 - 2284927, E-mail: directornitap@gmail.com

SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Education	NATIONAL INSTITUTE OF TECHNOLOGY, ARUNACHAL PRADESH (ESTABLISHED BY MINISTRY OF HUMAN RESOURCE DEVELOPMENT, GOVT. OF INDIA)	Ethics
In GOD's own land, a fusion of scholastic students, innovative & motivated researchers & teachers and fast moving visionary leaders.	 COURSE STRUCTURE & SYLLABUS FOR M-TECH IN VLSI DESIGN & EMBEDDED SYSTEM	Steeping Stone and Sky reaching ladder to success
Research	PO-Yupia, Dist.-PapumPare, ArunachalPradesh,Pin-791112 PhNo:0360-2284801/2001582 FaxNo:0360-2284972 Email- nitarunachal@gmail.com	Service to Society



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Professor Chandan Tilak Bhunia, Ph.D [Engg.], FIETE, FIE(I), SMIEEE

DIRECTOR



FORWARD

To achieve the target of being a global leader in the field of Technical Education, there is some sort of time bound urgency to work quickly, massively and strongly, in respect of National Institute of Technology, Arunachal Pradesh being an “Institute of National Importance” (by an Act of Parliament) and being established only in three years back in 2010. I have therefore adopted a ‘B’ formula as stated below to achieve the primary goal of producing world class visionary Engineers and Exceptionally brilliant Researchers and Innovators:

B- FORMULA

- Best for Teaching
- Best for Research
- Best for Entrepreneurship & Innovation
- Best for Services to Society

In implementing the ‘B’ formula in letter and spirit, the framing of syllabi has been taken as important legitimate parameter. Therefore, extraordinary efforts and dedications were directed for the last one year to frame a syllabi in a framework perhaps not available in the country as of today.

Besides attention on ‘B’ formula institute has given considerable importance to the major faults of current Technical Education while framing the syllabus. The major stumbling blocks in Technical Education today are:

- I. The present system is producing “Academic Engineers” rather than “Practical Engineers”.
- II. The present system of education makes the students to run after jobs rather than making them competent to create jobs.
- III. There is lack of initiative to implement the reality of “Imagination is more important than knowledge”.

Taking due consideration of the findings made above, to my mind a credible syllabi has been framed in the institute in which the major innovations are introduction of:

- I. I-Course (Industrial Course) one in each semester at least one, which is targeted to be taught by the Industrial Expert at least up to 50% of its component.
- II. Man making and service to society oriented compulsory credit courses of NCC/NSS, values & ethics.
- III. Compulsory audit course on Entrepreneurship for all branches.



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- IV. Many add-on courses those are (non-credit courses) to be offered in vacation to enhance the employability of the students.
- V. Many audit courses like French, German, and Chinese to enhance the communication skill in global scale for the students.
- VI. Research and imagination building courses such as Research Paper Communication.
- VII. Design Course as "Creative Design".

Further, the syllabi has been framed **not to fit in a given structure as we believe structure is for syllabus and syllabus is not for structure. Therefore, as per requirement of the courses, the structure, the credit and the contact hours has been made available** in case to case.

The syllabus is also innovative as it includes:

- I. **In addition to the list of text and reference books, a list of journals and magazines for giving students a flexible of open learning.**
- II. **System of examination in each course as conventional examination, open book examination and online examination.**

Each course has been framed with definite objectives and learning outcomes. Syllabus has also identified the courses to be taught either of two models of teaching:

- I. **J.C.Bose model of teaching where practice is the first theory.**
- II. **S.N.Bose model of teaching where theory is the first practice.**

Besides the National Institute of Technology, Arunachal Pradesh has initiated a scheme of **simple and best teaching** in which for example:

- I. **Instead of teaching RL, RC and RLC circuit separately, only RLC circuit will be taught and with given conditions on RLC circuits, RL and RC circuits will be derived and left to the students as interest building exercise.**
- II. **Instead of teaching separately High Pass Filter, Band Pass Filter and Low Pass Filter etc.; one circuit will be taught to derive out other circuits, on conditions by the students.**

I am firmly confident that the framed syllabus will result in **incredible achievements, accelerated growth and pretty emphatic win over any other systems** and therefore **my students will not run after jobs rather jobs will run after my students.**

For the framing of this excellent piece of syllabus, **I like to congratulate all members of faculty, Deans and HODs in no other terms but "Sabash!"**.

Prof. Dr. C.T. Bhunia
Director, NIT, (A.P.)



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TEACHING GUIDELINES

In order to achieve the desired goal of excellence and innovations in each and every function of National Institute of Technology, Arunachal Pradesh and to implement 'B' Plan in totality, I call upon my distinguished members of Faculty to invest some of their valuable business time in doing Research on Teaching. In this context, I put forward the following general guidelines for teaching practices in the institute:

- 1) **J.C. Bose Model of Teaching:** As an example, In the Basic Electronics course instead of first teaching the colour codes of the resistors in a theoretical class, teacher may carry few resistors to class and note down on the blackboard the colours of resistors and their values. Thereafter, the teacher may ask the students to device the color code creating enthusiasm among students. Similarly, instead of teaching the characteristics of PN junction diode, teacher may guide the students in a laboratory to draw the characteristics curve, then may advise the students to analyse the behaviour of characteristics. Thereafter, the teacher may teach the theory of PN junction diode.
- 2) **S.N. Bose Model of Teaching:** This is the conventional model of teaching where theory is first practice but even then I suggest some unique ideas to improve imaginative power and creativity of students in the subject. For example, instead of teaching two algorithms for conversion of decimal to binary, one for integral part and another for fractional part, I call upon the teachers to design a single algorithm for both the purposes for inspiring teaching.
- 3) I also believe that noble teaching **will be simple and in simpler way**. Therefore, I call upon the teachers not to teach bandpass filter, low pass filter, high pass filter separately. Teachers may design a single circuit for all filters and put on condition there on can derive separately circuits for separate filters. Similarly, instead of teaching RL, RC and RLC circuits separately, I call upon the teachers to teach only RLC circuit and then putting suitable condition on RLC circuit; RL and RC circuits may be derived and taught.
- 4) **Last but not the least**, I call upon the teachers to **solve all the problems of all chapters of the main text book prescribed for a subject** in a teaching-learning process – 50% to be solved by teachers (may be of even ones) and 50% may be solved by students (may be odd ones).

I solicit and anticipate full cooperation from all my brilliant pool of young and energetic faculty members to practice the noble and novel teaching procedures explained above without fail. Once procedures implemented by teachers are documented, we may proceed to file a patent on Research in Teaching on behalf of NIT, Arunachal Pradesh.

Prof. Dr. C.T. Bhunia
Director, NIT, (A.P.)



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In recent years, Electronics & Communication Engineering has made unprecedented growth in terms of new technologies, new ideas and principles resulting in extremely high rate of obsolescence of technologies. Researchers, academicians, industries and the society at large have to work in unison to meet the challenges of the rapidly growing discipline. The research organizations and industries that work in this frontier area are in need of highly skilled and scientifically oriented manpower. This manpower can be available only with flexible, adaptive and progressive training programs and a cohesive interaction among the research organizations, academicians and industries. The teaching program contains a proper blend of basic concepts and advances in technology. The faculty has succeeded in keeping a lively atmosphere among the students with innovative teaching techniques. The teaching is closely coupled with the research activities of the department. The ECE Department of NIT Arunachal Pradesh has been consistently working towards this goal. The Department of Electronics & Communication Engineering was established right from inception of the institute in 2010. The department offers a four year degree program in Electronics & Communication Engineering with an annual intake of 30 students & Doctoral program starts in 2013 July session. During these years, this department has diversified its activities in teaching and research. A continuous effort has been put forward towards setting up new laboratories and improves the facilities in the existing laboratories. Following are the laboratories developed with modern infrastructural facilities.

1. Advance Electronic Device & Circuit Lab
2. Electronics Measurement Lab
3. Modern Communication Engineering Lab
4. Embedded System Design Lab
5. Antenna & Propagations Lab
6. Microwave Engineering Lab
7. Digital Signal Processing Lab
8. Simulation Lab

At present research and development activities of department are in the following area:

1. Digital Signal and Image Processing
2. Microwave Patch Antenna
3. VLSI (Very Large Scale Integrated Circuit)
4. Mobile Communication
5. Microcontrollers based systems design.
6. Semiconductor Physics.

It is our objective to prepare our students to be successful in integrating all the field of engineering and science and to be able to pursue advanced studies in electronics engineering on a competitive global basis. The mission is a culmination of our effort to meet the mission of NIT Arunachal Pradesh, North East region and the nation at large.

1st year the student of ECE department learn about Basic Engineering subject with NCC and one Audit course of French / Korean and German / Chinese which meet Global Standard. 2nd and 3rd year student also have Audit course which help to prepare them to face the challenged in Industry. Syllabus also include Industrial Trainings and Project work which help student to fit into industry and research area.



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

SEMESTER – I

Subject Code	Subject	L	T	P	Credit
ECE 951	Physics of Semiconductor Devices	3	0	0	3
ECE 952	Digital VLSI Design	3	1	0	4
ECE 953	Analog & Mix-Signal Design	3	1	0	4
ECE 954	VLSI Technology	3	0	0	3
MAS 901	Advanced Mathematics for VLSI	3	1	0	4
ECE 955	VLSI Lab – I (HDL and FPGA based experiments)	0	0	4	2
ECE 956	VLSI Lab – II (SPICE/IRSIM/ MAGIC/ TCAD/ PROCESS based experiments)	0	0	4	2
Total		15	3	8	22

SEMESTER – II

Subject Code	Subject	L	T	P	Credit
ECE 961	Embedded System and RTOS	3	0	2	4
ECE 962	Algorithm for VLSI Design	3	0	0	3
ECE 963	Advanced Microcontrollers	3	0	0	3
ECE 964	VLSI System Design	3	0	0	3
ECE 9XX	Elective – I	3	0	0	3
ECE 965	System Design Lab (This lab would run on two days. One day for VLSI domain experiments and on the second day embedded system based experiments. (FPGA, uC, FPGA+uC or Hybrid arch., Std. Cell based, targeting towards tapeout)	0	0	8	4
ECE 966	Seminar	0	4	0	4
Total		15	4	10	24

SEMESTER – III

Subject Code	Subject	L	T	P	Credit
ECE 971	Pedagogy Practices	0	0	8	4
ECE 972	Microelectronics Technology Lab	0	0	8	4
ECE 973	Mini Project	0	0	8	4
ECE 974	M. Tech. Thesis (Preliminary)	0	0	8	8
Total		0	0	32	20

SEMESTER – IV

Subject Code	Subject	L	T	P	Credit
ECE 981	M. Tech. Thesis (Final)	0	0	24	24
Total		0	0	24	24



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Elective Paper – I

Subject Code	Subject	L	T	P	Credit
ECE 941	MEMS and Microsystems	3	0	0	3
ECE 942	Low Power VLSI Design	3	0	0	3
ECE 943	RF IC Design	3	0	0	3
ECE 944	Memory Subsystem Design	3	0	0	3
ECE 945	Advanced Digital Signal Processing	3	0	0	3
ECE 946	Testing and Verification	3	0	0	3



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Name of the Module: Physics of Semiconductor Devices

Module Code: ECE 951

Semester: 1st

Credit Value: 3 [L=3, T=0, P=0]

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet with the objectives of:

1. Imparting theoretical and practical knowledge to the students in the area of Heterostructure.
2. Providing teaching and learning to make students acquainting with advanced semiconductor devices.
3. Injecting the future scope and the research direction in the discipline of HBT & HEMT.

B. Learning Outcomes:

Upon completion of the subject:

1. Students will be adequately trained to research on HBT & HEMT.
2. Students will be skilled both theoretically and practically to use this subject for the application in wireless communication, optical communication and computers.

C. Subjects Matter:

UNIT - I

Semiconductor fundamentals: Band theory, E-k diagram, effective mass, density of states, statistics, carrier density, degeneracy, compensation. (4)

Transport: Ohm's law, mobility, Boltzmann equation, Hall mobility, diffusion, scattering mechanisms, hot electrons. (3)

Excess carriers: Recombination in direct gap, SRH theory, traps, continuity equation. (3)

P-N Junction theory: Band diagram of semiconductor P-N junction, depletion width, built-in potential, I-V characteristics, varactor diode. (3)

UNIT - II

Bipolar junction transistors: minority carrier distribution and terminal currents, generalized biasing, switching, secondary effects, frequency limitations of transistors. (4)

MOS Capacitors and MOSFETs: Band diagram under depletion, inversion and accumulation, threshold voltage and its control; C-V curves; I-V characteristics, gradual channel approximation, charge sheet model, Pao-Sah current formulation, subthreshold current conduction, channel length modulation; hot electrons. (8)

UNIT - III

Advanced MOSFETs: CMOS scaling, short channel effects, threshold voltage roll-off, DIBL, GIDL, gate leakage current, hot carrier injection, punch through, silicon-on-insulators (SOI) MOSFETs, low power and high speed design issues. (8)

UNIT - IV



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Heterostructures and Quantum Well Devices: Quantization and low dimensional electron gas, influence on MOSFET characteristics, band alignment in Si/SiGe heterostructures, high electron mobility transistors (HEMTs), Quantum Well FETs. (7)

D. Teaching/Learning/Practice Pattern:

Teaching: 70%

Learning: 30%

Practice: 0%

E. Examination Pattern:

Theoretical Examination: Regular Written Examination

F. Reading List:

BOOKS:

1. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 6th Edition, PHI Private Limited, 2011.
2. P. Bhattacharya, Semiconductor Optoelectronics Devices, 2nd Edition, PHI, 2009.
3. G. Massobrio and P. Antognetti, Semiconductor Device Modeling with SPICE, 2nd Edition, TMH, 2010.
4. C. C. Hu, Modern Semiconductor Devices for Integrated Circuits, Pearson Education, 2010.
5. R. S. Muller and T. I. Kamins, Device Electronics for Integrated Circuits, 3rd Edition, Wiley India, 2009.
6. S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd Edition, Wiley India, 2010.
7. Y. Tsididis, Operation and Modeling of the MOS transistor, 2nd Edition, TMH, 1999.
8. S. A. Neamen and D. Biswas, Semiconductor Physics and Devices, 4th Edition, TMH, 2012.

B. MAGAZINES:

1. IEEE magazines on Semiconductor manufacturing.
2. IEEE Solid State Circuits Society newsletter.

C. Journals:

1. IEEE transactions on solid states circuits
2. IEEE transactions on VLSI
3. Journal of Circuits, systems and computers, world scientific publisher
4. Applied Physics Letter
5. Journal of Nanoscience and Nanotechnology.



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Name of the Module: *Digital VLSI Design*

Module Code: *ECE 952*

Semester: *1st*

Credit Value: *4 [L=3, T=1, P=0]*

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet with the objectives of:

1. To introduce students to basic concepts of digital VLSI chip design using the simpler VLSI technology.

B. Learning Outcomes:

Upon completion of the subject:

1. An ability to design logic circuit layouts for both static CMOS and dynamic clocked CMOS circuits.
2. An ability to extract the analog parasitic elements from the layout and analyze the circuit timing using a logic simulator and an analog simulator.
3. An ability to build a cell library to be used by other chip designers.
4. An ability to insert elementary testing hardware into the VLSI chip.
5. An ability to analyze VLSI circuit timing using Logical Effort analysis.
6. An ability to design elementary data paths for microprocessors, including moderate-speed adders, subtracters, and multipliers.
7. An ability to estimate and compute the power consumption of a VLSI chip.
8. An ability to assemble an entire chip and add the appropriate pads to a layout
9. An ability to explain the chip technology scaling process.

C. Subjects Matter:

UNIT - I

VLSI Physical Design concepts: CMOS VLSI fabrication, Concept of Mask design, Mask layout, Design rules and DRC, Stick diagram, Standard cell vs Custom design. (4)

Introduction to Logic Design: Logic implementation using switches, Transistors as switches, Concept of 'strong' and 'weak' signals, CMOS architecture, Designing static CMOS Logic circuits. (4)

The CMOS Inverter: Steady state IO characteristic, Noise margin, Tuning the characteristic; Regenerative properties; CMOS latch-up; CMOS power dissipation mechanisms (4)

UNIT – II

CMOS combinatorial logic design: R-C calculation – delay analysis; Logical effort and electrical effort. Driving large fan-outs. Speed and power dissipation; Technology scaling. (5)

Other MOS Logic Circuits: n-MOS, p-MOS and pseudo NMOS Logic, Ratioed vs. Ratio less logic; Dynamic CMOS Logic – static vs. dynamic CMOS, speed and power dissipation, charge leakage, charge sharing clock feed through and cascading issues, domino logic and n-p CMOS; Pass transistor logic and transmission gates. (5)

UNIT - III

Interconnects: Parameters – C, R, L. Electrical wire models – lumped vs. distribute R-C lines; Elmore delay model, wire model, Buffers and their placement; (5)



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Arithmetic and Logic Circuits: Adder circuits – Carry Look-ahead Adder, Carry Select Adder, Multipliers, Barrel Shifters, General purpose functional blocks and ALU Design. (5)

UNIT – IV

Sequential circuits: Synchronous and Asynchronous circuits; Concept of Finite State Machine (FSM), Moore and Mealy machines, Synchronous FSM Design, State Diagram, State Assignment, Derivation of ‘Next State’ and ‘Output’ expressions. (5)

Latches and Registers: Static and dynamic latches and registers, The Master-slave concept Timing metrics, Effect of clock skew and jitter, sources of clock skew and jitter; Clock generation and distribution in VLSI chips. (5)

D. Teaching/Learning/Practice Pattern:

Teaching: 70%

Learning: 30%

Practice: 0%

E. Examination Pattern:

Theoretical Examination: Regular Written Examination

F. Reading List:

BOOKS:

1. J.M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits- A Design Perspective, 2nd ed., PHI, 2003
2. S.M. Kang and Y. Leblevici, CMOS Digital Integrated Circuits Analysis and Design, 3rd ed., McGraw Hill, 2003
3. J. P. Uyemura, CMOS Logic Circuit Design, Springer
4. David A. Hodges, Horace G. Jackson, R. A. Saleh, Analysis and Design of Digital Integrated Circuits, McGraw-Hill Series in Electrical and Computer Engineering, Aug 2003

B. MAGAZINES:

- 1.

C. JOURNALS:

1. Integration, the VLSI Journal
2. IEEE Transactions on Very Large Scale Integration (VLSI) Systems



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Name of the Module: Analog and Mixed Signal Design

Module Code: ECE 953

Semester: 1st

Credit Value: 4 [L=3, T=1, P=0]

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet with the objectives of:

1. to complement the student VLSI background acquired in the previous core courses on electronics, stressing on important advanced concepts and providing designer insight in the area of VLSI analog and mixed-signal design.
2. Second, to introduce the critical issues to take into account in the full design of a mixed-signal, submicron/nanometer-scale integrated circuit.

B. Learning outcomes:

Upon completion of the subjects:

1. Explain the basic design concepts for low power mixed signal VLSI circuits in CMOS technology.
2. Apply the knowledge in low-power analog and mixed-signal VLSI circuit analysis and simulation.
3. Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance.
4. Design low-power analog and mixed-signal VLSI circuits by using CMOS processes.

C. Subject Matter:

UNIT – I

Introduction: Signals, Frequency Spectrum of signals, Analog and Digital signals, Amplification of signals. (1)

Review of MOS Transistor: Small signal and large signal equivalent circuit, MOS capacitance model, High frequency equivalent circuit; Sub-threshold MOS operation, MOS SPICE models, SPICE simulation of MOS circuits (3)

Amplifiers: Transistor amplifiers, Common Source (CS), Common gate (CG) and Common drain (CD) configurations; Principle of amplification, Load line and Transfer characteristics, Linear and non-linear regions, Importance of Biasing; Transistor biasing in VLSI circuits, Current sources and current mirrors. (5)

UNIT - II

Quantitative analysis: Amplifier equivalent circuit, low frequency analysis of CS, CG and CD amplifiers; High frequency equivalent circuit, frequency response, Miller effect and Miller capacitance, Bode plot, concept of stability, stability analysis, comparison of CS and CG circuit performance. (5)

Cascode Amplifiers: Basic cascode configuration, Gain/bandwidth tradeoff; VLSI implementation– signal swing vs supply voltage limitation, folded cascode configuration. (5)

UNIT - III

Differential and multi-stage amplifiers: The MOS differential pair, differential gain, common mode gain and CMRR, importance of transistor matching, VLSI layout techniques for transistor matching; Differential to single ended conversion. (4)



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CMOS Operational Amplifiers: Basic concepts of Op-Amp; Performance Parameters; One stage Op-amp; Two stage Op-amp; Stability and Phase compensation; Cascode Op-amp; Design of Two stage and Cascode Op-amp; SPICE simulation of Amp; High performance CMOS Op-amps; Micropower Op-amp; Low noise Op-amp; Low voltage Op-amp; Design Examples. (4)

Switched capacitors circuits: General considerations; Switched capacitor integrators; First and second order switched capacitor filter circuits; Design examples. (4)

UNIT - IV

Comparators: Characterization, Two state open loop comparators; Discrete time comparators; high speed comparators circuits; CMOS Sample and hold circuits; Design examples. (3)

Data Converter Fundamentals: Ideal D/A converters, Ideal A/D converter; Serial and Flash D/A converters and A/D converters; Medium and High Speed converters; Over-sampling converters, Performance limitations; Design consideration. (6)

D. Teaching/Learning/Practice Practice Pattern:

Teaching: 70%

Learning: 30%

Practice: 0%

E. Examination Pattern:

Theoretical Examination: Open book/ Regular examination and on line test.

F. Reading List:

BOOKS:

1. Adel Sedra, Kenneth C. Smith, Microelectronic Circuits, The Oxford Series in Electrical and Computer Engineering
2. R. Jacob Baker, Harry W. Li, David E. Boyce, Cmos: Circuit Design, Layout, and Simulation, IEEE Press Series on Microelectronic Systems
3. Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, The Oxford Series in Electrical and Computer Engineering, 2002

MAGAZINES:

- 1.

JOURNALS:

1. Analog Integrated Circuits and Signal Processing
2. Circuits and Systems I: Regular Papers, IEEE Transactions on
3. Electron Device Letters, IEEE
4. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on



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Name of the Module: VLSI Technology

Module Code: ECE 954

Semester: 1st

Credit Value: 3 [L=3, T=0, P=0]

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet with the objectives of:

1. This course introduces the theory and technology of micro/nano fabrication. Because of the interdisciplinary nature of the subject, its content includes concepts from many disciplines in engineering (electrical, materials, mechanical, chemical) and science. In lecture, we will discuss the theory of basic processing techniques, such as diffusion, oxidation, photolithography, chemical vapor deposition, physical vapor deposition, etching, and metallization.
2. In the labs section of this course, we will be fabricating three different devices; an MOS capacitor, a microcantilever, and a microfluidic device. You will test each device in the lab and prepare a laboratory report for each device.
3. At the end of this course, one should have a good understanding of the various processing techniques used to micro/nano fabricate. One should understand the theory of the individual processes, how they are characterized, and the interrelationship of these processes when combined to fabricate devices.

B. Learning outcomes:

Upon completion of the subjects:

1. To develop knowledge and an understanding of micro and nano fabrication technologies, processes and their applications
2. appreciate the difference between micro- and nano-fabrication in the context of CMOS scaling
3. describe a range of nanoscale fabrication and characterisation technologies
4. demonstrate understanding of specific nanofabrication approaches
5. explain image formation in a number of high-resolution microscopies
6. identify some major issues and developments at the frontiers of nano-engineering

C. Subject Matter:

UNIT – I

Wafer Fabrication: Crystal structure, Defects in crystals, Silicon purification, Czochralski and Float Zone Crystal growth methods, dopant incorporation, wafer preparation. (5)

Metrology: Resistivity and Hall effect, Van der Pauw technique, microscopy and defect etches, optical characterization of thin films, ellipsometry, FTIR. (5)

UNIT – II

Diffusion: Solid solubility, diffusion equation and its solutions, drive-in diffusion, measurement methods I-V, C-V, ECV profilometry, SIMS. (5)

Ion Implantation: Equipment for implantation in silicon, Crystal structure and channeling, ion stopping mechanisms, damage production, annealing, different Ion implanter configurations, models and simulation. (5)



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

UNIT – III

Thermal Oxidation: Equipment for Oxidation, dry and wet oxidation, oxidation kinetics, linear parabolic model of thermal oxidation, the Si/SiO₂ interface. (6)

Thin film deposition for VLSI: PVD, metallization and sputtering, APCVD, LPCVD, deposition of epitaxial silicon, polysilicon, silicon dioxide and silicon nitride, PECVD, deposition of refractory metals, silicide formation. (6)

UNIT – IV

Photolithography: Light sources, wafer exposure systems, photoresists, alignment, mask design, limits to optical photolithography. (5)

Process integration: Clean room concepts, current trends in nanoscale fabrication. (5)

D. Teaching/Learning/Practice Practice Pattern:

Teaching: 70%

Learning: 30%

Practice: 0%

E. Examination Pattern:

Theoretical Examination: Open book/ Regular examination and on line test.

F. Reading List:

BOOKS:

1. J. D. Plummer, M. D. Deal and P. B. Griffin, Silicon VLSI Technology, Fundamentals, Practice and Modeling, Pearson education, 2000.
2. Dieter K. Schroder, Semiconductor Material and Device Characterization, 2006
3. S. A. Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 1996.
4. G. S. May and S. M. Sze, Fundamentals of Semiconductor Fabrication, Wiley India, 2004.
5. S. M. Sze, VLSI Technology, 2nd Edn., TMH, 2004.
6. M. J. Madou, Fundamentals of Microfabrication, 2nd Edition, CRC Press, 2011.

MAGAZINES:

1. IEEE Magazine for Consumer Electronics
2. I-Micronews
3. Magazine on Solid state Technology
4. CMM internationals

JOURNALS:

1. IEEE journal of Micro-electromechanical Systems.
2. Journal of Micro / Nanolithography, MEMS and MOEMS
3. Journal of Microlithography, Microfabrication, and Microsystems
4. Microsystems Technology
5. IEEE International Conference on Solid State Sensors and Actuators Transducers



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: Advanced Mathematics for VLSI

Module Code: MAS 901

Semester: 1st

Credit Value: 3 [L=3, T=0, P=0]

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet with the objectives of:

1. To gather knowledge on differential equations, simple integrals, special functions.
2. To work linear partial differential equations, diffusion, wave.

B. Learning outcomes:

Upon completion of the subjects:

1. Understand higher order differential equations, green functions.
2. Knowledge about oscillatory integrals, evaluating integral transforms.

C. Subject Matter:

UNIT – I

Combinatorics-1

Introduction to Combinatorics: Binomial Coefficients, Multinomial Coefficients, The Pigeonhole Principle, Concepts of Inclusion and Exclusion. (3)

Generating Functions: Double Decks, Counting with Repetition, Changing Money, Fibonacci Numbers, Catalan Numbers. (4)

Recurrence Relation: Linear recurrence relations with constant coefficients (linear and non-linear case), discussion of several cases to obtain particular solutions, Solution of linear recurrence relations using generating functions. (3)

UNIT – II

Combinatorics-2

Theory of Counting: Permutation Groups, Burnside's Lemma, The Cycle Index, Poly's Enumeration Formula, de Bruijn's Generalization. (4)

Network Algorithms: Gale-Shapley Algorithm, Concept of Stable Marriage and its variations. Combinatorial Geometry: Sylvester's Problem, Convex Polygons. (4)

Infinite Combinatorics: ZFC, Ordinals, Cardinals, Incompleteness and Cardinals, Weakly Compact Cardinals, Finite Combinatorics with Infinite Consequences. (4)

UNIT – III

Graph Theory

Introduction to Graph Theory: Graphs and their Relatives, Distances in Graphs, Graph Models and Distances, Cycles, paths, handshaking theorem, bipartite graph, Sub- Graph, planar graphs, Graph Isomerism, Operation on Graphs, Matrices related with Graphs. (4)

Tree: Properties of Trees, Matrix Tree Theorem, Tree Transversal, Spanning Trees, Counting Trees. (3)

Circuits, Paths and Cycles: Eulerian Trails and Circuits, Hamiltonian Graphs, Eulerian Formula, Bridges of Konigsberg, Stereographic Projection. (3)



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Colorings, Matching and Ramsey Theory: Chromatic Number and Polynomials, Hall's Theorem and SDRs, Konig-Egervary Theorem, Ramsey Numbers and Bounds, Graph Ramsey Theory. (4)

UNIT – IV

Linear Algebra.

Linear Systems, Vector Spaces and Determinants: Gauss's Method, Describing Solution Set, Linear Geometry, Gauss-Jordan Reduction, Linear Combination Lemma, Definition of vector space, Linear Independence, basis and Dimensions, Combining Subspaces. Determinants: Definition, Geometry of Determinants, Laplace's Formula. (4)

Maps Between Spaces: Isomorphism, Homomorphism, Computing Linear Maps, Matrix Operations, Nilpotence Matrix, Change of Basis, Projection, Geometry of Linear Maps, Markov Chains, Direct Sum Decomposition and Projection Operators, The Dual Space, Subspace Annihilators, Inner product spaces, Orthonormal bases, Gram- Schmidt process, Orthogonal Complementary Subspaces. (4)

Theorems: Primary Decomposition Theorem and Jordan Decomposition, Cyclic Decomposition, Bessel's Inequality, Parseval's Identity, Least Squares Solutions, Projection Theorem, Spectral Theorem. (Pre-requisite: Eigenvalues and Eigenvectors of Linear Operators, Unitary Operators Diagonalization of Linear Operators, Minimal Polynomial, Cayley- Hamilton theorem). (4)

D. Teaching/Learning/Practice Practice Pattern:

Teaching: 40%

Learning: 10%

Practice: 50%

E. Examination Pattern:

Theoretical Examination: Open book/ Regular examination and on line test.

F. Reading List:

BOOKS:

1. Kenneth H. Rosen, Discrete Mathematics and Its Applications, Tata McGraw - Hill Education
2. R. A. Brualdi, "Introductory Combinatorics," Pearson, 2009.
3. Discrete Mathematical Structures With Applications to Computer Science, Jean-paul Tremblay, McGraw-Hill
4. Narsingh Deo, Graph Theory With Applications To Engineering And Computer Science, PHI Learning
5. F. Harary, Graph Theory, Narosa Publishing House
6. David C. Lay, Linear Algebra and its Applications, Pearson India
7. Gilbert Strang, Introduction To Linear Algebra, Cambridge University Press
8. Gilbert Strang, Linear Algebra and its Applications, Cengage Learning



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: *VLSI Lab –I (HDL and FPGA based experiments)*

Module Code: *ECE 955*

Semester: *1st*

Credit Value: *2 [L=0, T=0, P=4]*

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet with the objectives of:

1.

B. Learning outcomes:

Upon completion of the subjects:

1.

C. Subject Matter:

UNIT – I

Introduction to HDL – Basic Concepts, Hierarchical Modeling Concepts, Modules, Ports, Gate-Level/Dataflow/Behavioural Modeling Concepts, Tasks, Functions (12Hrs)

Advance HDL Concepts – Timing and Delays, Switch-Level Modeling, User-Defined Primitives, Programming Language Interface, Logic Synthesis with HDL (Self Study)

UNIT – II

Lab Assignments

(36 Hrs)

- Hands on experience of Xilinx ISE or Altera Quartus
- Designing basic building blocks (logic blocks, counter, registers etc.)
- Design of a multibit adder circuits
- Design of multibit unsigned/signed fixed/floating multiplier
- Design of multibit unsigned/signed fixed/floating divider
- Course Project



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: VLSI Lab – II (TCAD/ PROCESS/SPICE/IRSIM/ MAGIC based experiments)

Module Code: ECE 956

Semester: 1st

Credit Value: 2 [L=0, T=0, P=4]

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet with the objectives of:

1.

B. Learning outcomes:

Upon completion of the subjects:

1.

C. Subject Matter:

UNIT – I

Introduction to Device Simulation

Sentaurus (Synopsys) device simulation overview and device design steps (4Hrs)

Process simulation using Sentaurus (4Hrs)

Lab Assignments (08 Hours)

- A complete CMOS Process flow will be covered in the laboratory sessions.
- Students will be asked to design a MOSFET and will be asked to develop BSIM1 and BSIM3 SPICE device models. These models will be used in circuit simulator while designing electrical circuits.

Home work: Design of FinFET at 18nm or lower technology node.

UNIT – II

Introduction to Circuit Simulation

Introduction to the Design Flow and Introduction to SPICE: SPICE Basics, Basic device models, Introduction to different analyses (OP, DC, TRAN, AC etc.) (4Hrs)

Lab Assignments (12 Hours)

- Hands-on session using various examples for different analyses. Beginning from an inverter design to the design of an 8-bit adder. Use of the device model developed during Unit – 1 of this course into the circuits being designed in Unit – 2 for the study of performance study of circuits with respect to the device parameters.

Home work: One 16 bit signed multiplier, 8T- SRAM Cell Design, Low Noise Amplifier and PLL

UNIT – III

Introduction to Timing Analysis and Circuit Layout Techniques

Introduction to IRSIM and MAGIC(08 Hrs)

- Switch Level Circuit simulation using IRSIM
- Layout design using MAGIC
- Circuit Extraction in SPICE/IRSIM format and simulation
- Validation of pre-layout and post-layout simulation results



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Lab Assignments

(12 Hours)

- Hands-on session using various circuits such as amplifiers, logic blocks or digital circuits such as 16 bit counter etc.

Home work: One 16 bit signed multiplier, 8T- SRAM Cell Design layout in Magic and simulation in SPICE of extracted netlist



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: Embedded System & RTOS

Module Code: ECE 961

Semester: 2nd

Credit Value: 4 [L=3, T=0, P=2]

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet the objectives of:

1. Define the class and its goals
2. Provide a general overview of Embedded Systems
3. Learn to design and development of an embedded system, including hardware and embedded software development.
4. Give examples of Embedded Systems
5. Show current statistics of Embedded Systems

B. Learning outcomes:

Upon Completion of the subjects:

1. Know about Embedded systems and the interface issues related to it.
2. Know about different techniques on embedded systems
3. Know about the real time models, languages and operating systems
2. To analyze real time examples, obstacles and solutions.

C. Subject Matter:

UNIT - I

Introduction to Embedded systems. Embedded systems vs. general computing systems. Introduction to different embedded processors like 8051, ARM, PIC,DSP, FPGA based processors etc. Hardware/software co-design, co-design for system specification and modeling. Single-processor architectures and multi-processor architectures. The co-synthesis Problem. State transition graph. (10)

UNIT - II

Models of computation, requirements for embedded system specification, hardware/software partitioning problem, hardware/software cost estimation. Generation of partitioning using different modeling technique, external peripherals – types of memory and their management, case studies. (10)

UNIT-III

Introduction to RTOS: OS in embedded SoC. Introduction to tasks, process and threads. Muti-processing and multi-tasking. Task scheduling. Inter process communication, message passing, interrupt driven input and output – non-maskable interrupt, software interrupt. Threads – single, multi-thread concept; multitasking sequential circuit, task synchronization techniques. Handling of interrupts in RTOS and timing analysis. Case studies. (10)

UNIT-IV



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Embedded system modeling, embedded C, role of infinite loop, instruction sequencing, compiling, state machine, pattern sequence detector, different types of embedded multitasking sequential switching circuit design and optimization. Case studies. (10)

D. List of Practical:

1. Design an embedded controller for automatic room temperature control.
2. Design an FPGA based embedded SoC system.
3. Design an embedded system for industrial automation.
4. Design an embedded system for AUV.
5. Design an embedded system for Robot gripper.
6. Design an embedded system for wheel mechanism of mobile robot.
7. Design an embedded system for obstacle avoidance by an assembly line robot.
8. Any innovative embedded system design as mini project.

E. Teaching/ Learning/ Practice Pattern:

Teaching: 30%

Learning: 20%

Practice: 50%

F. Examination Pattern:

Theoretical Examination: Regular Examination

G. Reading List:

TEXT BOOK

1. W. Wolf, "Computers as components: Principles of embedded computing system design", 2/e, Elsevier, 2008.
2. R. Gaonkar, "Fundamentals of Microcontrollers and Application in Embedded Systems," Penram International Publishing, 2015
3. A. N. Sloss, D. Symes, and C. Wright, "ARM system developer's guide: Designing and optimizing system software", Elsevier, 2008.

REFERENCES

1. Product data sheet LPC 2141/42/44/46/48. NXP Semiconductors.
2. ARM7TDMI Technical Reference Manual, ARM Limited.
3. Jack Ganssle, "The art of designing embedded systems", 2/e, Elsevier, 2008.
4. Michael Barr, "Programming Embedded Systems in C and C++", O'Really, 1999.
5. Kirk Zurell, "C Programming for Embedded Systems", CMP Books, 2000.
6. Muhammod Ali Mazidi, Rolin D. Mckinlay & Danny Sansey, "PIC Microcontroller and Embedded System Using Assembly & C for PIC18," Pearson International Edition, 2008.
7. Muhammod Ali Mazidi, Janice Gillispie Mazidi & Rolin D. Mckinlay, "The 8051 Microcontroller and Embedded System Using Assembly & C," Pearson India.

MAGAZINES:

1. Embedded Systems Design magazine archive, South Tower San Francisco, CA 94107
2. Embedded Innovator Newsletter and magazines, Intel, Santa Clara, CA.
3. Embedded Computing Design, Saint Clair Shores, MI 48082
4. AI Magazine - Association for the Advancement of Artificial Intelligence, AAAI Press, USA



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

5. IEEE Intelligent Systems Magazine, Computer Society, United State

JOURNALS:

1. International Journal of Embedded Systems, Inder Science Publishers, ISSN online: 1741-1076, ISSN print: 1741-1068
2. International Journal of Reconfigurable and Embedded Systems (IJRES), ISSN: 2089-4864, IAES
3. Journal of Embedded Computing, ISSN 1740-4460, IOS Press
4. Journal of Embedded Systems, Science and Education Publishing.
5. Applied Soft Computing - Journal - Elsevier, Netherland



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: *Algorithms for VLSI Design*

Module Code: *ECE 962*

Semester: *2nd*

Credit Value: *3 [L=3, T=0, P=0]*

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet the objectives of:

1. Define the class and its goals

B. Learning outcomes:

Upon Completion of the subjects:

1. Know about Embedded systems and the interface issues related to it.

C. Subject Matter:

UNIT - I

VLSI Design Cycle: Design problem and design domains, levels of abstractions like algorithmic and system design, structural and logic design, transistor level design, layout design. Y diagram. Design flow for digital and analog VLSI design. (2)

Graph Algorithms and Computational Complexity: Basic definitions and data structures for representations of graphs, Examples of graph algorithms like depth-first search, breadth-first search, Dijkstra's algorithm, computational complexity, complexity classes, NP completeness and NP hardness. (10)

UNIT - II

VLSI design simulations: Basic concepts and purpose of simulations, Gate-level modeling and simulations, compiler-driven simulation and event-driven simulations, Transistor-level modeling and simulation. (3)

High-level Synthesis: Hardware models for high-level synthesis, data flow graph, simple, conditional and iterative data flow, data flow graph representations, ideas of allocation, assignment and scheduling. (4)

Logic level synthesis and verifications: Introduction to combinational logic synthesis, binary decision diagrams, ROBDD, two-level logic synthesis. (5)

UNIT-III

Partitioning and Floor planning: Problem formulations, classification of partitioning algorithms, Kernighan-Lin Algorithm, basic ideas of floor planning problem. (5)

Placement and Routing: Basic concept, problem formulation and algorithms of placement, global routing, detailed routing, channel routing algorithm, maze routing algorithms. (5)

UNIT-IV

Electronic design automation: Basic ideas and purpose, examples of commercially available EDA tools, computer-aided analog designs. (6)



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

D. Teaching/ Learning/ Practice Pattern:

Teaching: 70%

Learning: 30%

Practice: 0%

E. Examination Pattern:

Theoretical Examination: Regular Examination

F. Reading List:

TEXT BOOK

1. Algorithms for VLSI Design Automation by S. H. Gerez, John Wiley & Sons. Ltd., England (1999).
2. Algorithms for VLSI Physical Design Automation by Naveed Sherwani, Kluwer Academic Publishers, New York (2002).

MAGAZINES:

- 1.

JOURNALS:

1. Integration, the VLSI Journal - Elsevier



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the module: *Advanced Microcontrollers*

Module Code: *ECE 963*

Semester: *2nd*

Credit Value: *3 [L=3, T=0, L=0]*

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet the objectives of:

1. Provide a general overview of Embedded Systems and different embedded processor.
2. Learn to design and development of the real-time system.
3. Learn to hardware and software partition, co-design and verification.
4. Real-time embedded systems design

B. Learning outcomes:

Upon Completion of the subjects:

1. Know about Embedded systems and the interface issues related to it.
2. Know how the real-time systems are model and analysis.
3. Students can analyze real-time system and different design constraints

C. Subject Matter:

UNIT - I

Review of basic concepts, architecture, functioning and instruction set of 8085 microprocessor. Polling and interrupt. RISC and CISC Architectures; Difference between RISC and CISC. (05)

UNIT - II

Introduction to 8051 architecture and programming model. Internal RAM and registers, special function registers. I/O ports, 8051 addressing modes, arithmetic and logic instructions and programming. 8051



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programming in C. Timer/counter programming and serial port programming. Interrupt system and instruction sets. Case studies (08)

UNIT- III

Introduction to PIC microcontrollers. Architecture and memory organization. Assembly language programming. Registers, I/O port programming, arithmetic and logic instructions. PIC programming in C. Interrupts, timer, ADC, DAC, sensor interfacing. Compare mode programming and capture mode programming. SPI bus protocol. Instruction sets. Case studies (10)

UNIT- IV

Introduction to ARM processor family. Introduction to the development of microprocessor based products. Overview of the design process, preparing the specifications, development of a design, Implementation and testing. Regulatory compliance testing, Introduction to design tools for microprocessor development. (07)

Development of ARM architecture, instruction pipeline, interrupts and vector table. Introduction to ARM programming model, ARM instruction set and C programming for ARM. Memory management. Case studies using Raspberry Pi, Intel Galileo or Edison microprocessors for Embedded System and IoT. (10)

D. Teaching/ Learning/ Practice Pattern:

Teaching: 70%

Learning: 30%

E. Examination Pattern:

Theoretical Examination: Regular Examination

F. Reading List:

TEXT BOOK

1. W. Wolf, "Computers as components: Principles of embedded computing system design", 2/e, Elsevier, 2008.
2. Kenneth Ayala, "The 8051 Microcontroller", Thomson, New Delhi, 2005.
3. Muhammod Ali Mazidi, Rolin D. Mckinlay & Danny Sansey, "PIC Microcontroller and Embedded System Using Assembly & C for PIC18," Pearson International Edition, 2008.
4. A. N. Sloss, D. Symes, and C. Wright, "ARM system developer's guide: Designing and optimizing system software", Elsevier, 2008.

REFERENCE BOOKS:

1. Muhammod Ali Mazidi, Janice Gillispie Mazidi & Rolin D. Mckinlay, "The 8051 Microcontroller and Embedded System Using Assembly & C," Pearson India.
2. Product data sheet LPC 2141/42/44/46/48. NXP Semiconductors.
3. ARM7TDMI Technical Reference Manual, ARM Limited.
4. Jack Ganssle, "The art of designing embedded systems", 2/e, Elsevier, 2008.
5. Michael Barr, "Programming Embedded Systems in C and C++", O'Really, 1999.
6. Kirk Zurell, "C Programming for Embedded Systems", CMP Books, 2000.

MAGAZINES:

1. Embedded Systems Design magazine archive, South Tower San Francisco, CA 94107
2. Embedded Innovator Newsletter and magazines, Intel, Santa Clara, CA.



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

3. Embedded Computing Design, Saint Clair Shores, MI 48082
4. AI Magazine - Association for the Advancement of Artificial Intelligence, AAAI Press, USA
5. IEEE Intelligent Systems Magazine, Computer Society, United State

JOURNALS:

1. International Journal of Embedded Systems, Inder Science Publishers
2. International Journal of Reconfigurable and Embedded Systems (IJRES)
3. Journal of Embedded Computing, IOS Press
4. Journal of Embedded Systems, Science and Education Publishing.
5. Applied Soft Computing - Journal - Elsevier, Netherland
6. Indian Journal of Science and Technology



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the module: *VLSI System Design*

Module Code: *ECE 964*

Semester: *2nd*

Credit Value: *3 [L=3, T=0, L=0]*

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet the objectives of:

1.

B. Learning outcomes:

Upon Completion of the subjects:

1.

C. Subject Matter:

UNIT - I

Basics of system hardware design: Hierarchical design using top-down and bottom-up methodology, System partitioning techniques, interfacing between system components; Programmable logic devices (FPGA, CPLD, PLA, PAL), Design phases (design, testing, fabrication, packaging), Abstraction and their types, computer aided designs(modeling, analysis, & simulation), VLSI design flow, ASIC design flow. (08)

UNIT - II

Designing basic building blocks: Digital systems design using conventional components such as gates, flip-flops, PALs, FPGAsetc.; Arithmetic Logic design, Designing multi data path ALU; Algorithmic State Machine; Memories: Introduction to different types of memories, single and multiple port memories; Introduction to GALS (Globally Asynchronous Locally Synchronous);Introduction to Network on Chip; Introduction to FIFO and designing fast FIFOs. (10)



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UNIT- III

Clocks: Static timing analysis; Handling multiple clock domains; Global and local clock distribution; Case Studies involving system designing using CAD tools around soft-core processors and other peripherals (I/O, Memories etc.) (10)

UNIT- IV

Processor Design: Von Neumann architecture, Harvard architecture, modified Harvard architecture. Datapath and Control, Enhancing performance with Pipelining, Exploiting Memory hierarchy. Case studies using Intel X86 family of advanced microprocessors, programming model for x86 family. 8086 microprocessor architecture, addressing modes, instruction set, assembly language programming. Stacks, micros, interrupts, interrupt service routines. 8086 system bus structure. I/O programming. Multiprocessor configurations, coprocessors. Memory and I/O interfacing. Parallel and serial communication interface. D/A and A/D interface, timers. Keyboard/display controller, interrupt controller, DMA controller. Hardware of 186, 286, 386, 486 & Pentium processors. Overview of Motorola 68XXX family of microprocessors, 68XXX addressing modes, instruction set, hardware. (15)

D. Teaching/ Learning/ Practice Pattern:

Teaching: 70%

Learning: 30%

E. Examination Pattern:

Theoretical Examination: Regular Examination

F. Reading List:

TEXT BOOK

1. D. A. Patterson and J. L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, 2nd Edition, Morgan Kaufmann Publishers, Inc, 1998.
2. J. Rabaey, Digital Integrated Circuits, A Design Perspective, 2nd Edition, Pearson Education, 2003.
3. Books on PLDs, books on Computer Architecture, Book by Bokaglu, Book by John P. Hays

REFERENCE BOOKS:

- 1.

MAGAZINES:

- 1.

JOURNALS:

- 1.



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: *System Design Lab*

Module Code: *ECE 965*

Semester: *2nd*

Credit Value: *4 [L=0, T=0, P=8]*

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet with the objectives of:

1.

B. Learning outcomes:

Upon completion of the subjects:

1.

C. Subject Matter:

Advanced Design Techniques using Commercial EDA Tools, FPGA and Embedded Processors
(Through this module, students will be introduced to VLSI Circuit Design Flow. The EDA tools covered in this module are chosen for this purpose only.)

1. Analog Schematic Editor/ Cadence Virtuoso OA (IC616) (04 Hrs)
2. VCS (Synopsys)/ HSpice / XA (Synopsys) (04Hrs)
3. VLSI Circuit Synthesis (Theory) (04 Hrs)
4. DC compiler (Synopsys) for Synthesis and DFT(04Hrs)
5. IC Compiler (Synopsys) for Digital Layout (Place and Route)(04Hrs)
6. Physical verification Calibre (Mentor Graphics) (DRC/LVS/XRC)(04Hrs)
7. ATPG TetraMax (Synopsys)(04Hrs)
8. STA PrimeTime (Synopsys)/ Prime Power/ Prime Rail(04Hrs)
9. FPGA and Embedded Processor (Using Soft Processor core on FPGA platform itself) Interfacing (08 Hrs)
10. FPGA and external processor interfacing (08 Hrs)

Lab Assignments: In the laboratory sessions, an 8-bit ALU will be designed in HDL which will be synthesized and layout will be generated for the further testing and verification. Finally a fabrication ready circuit will be the outcome for 180nm/65nm/ or lower technology node.

Home work: Design of a 16 bit CORDIC processor with the given set of instructions.



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Elective Paper – I

Subject Code	Subject	L	T	P	Credit
ECE 941	MEMS and Microsystems	3	0	0	3
ECE 942	Low Power VLSI Design	3	0	0	3
ECE 943	RF IC Design	3	0	0	3
ECE 944	Memory Subsystem Design	3	0	0	3
ECE 945	Advanced Digital Signal Processing	3	0	0	3
ECE 946	Testing and Verification	3	0	0	3



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: MEMS and Microsystems

Module Code: ECE 941

Semester: 2nd

Credit Value: 3 [L=3, T=0, L=0]

Module Leader:

No. of Lectures:

A. Objectives:

The course is designed to meet with the objectives of

1. To give them hands on experience for the fabrication processes using micro-fabrication tools In the cleanroom.
2. Briefly review on various application fields of the microsensors, MEMS, and smart devices.
3. The materials and the processes required to make different kinds of the microdevices.
4. The standard microelectronics technology to produce ultra large-scale integrated circuits and package them will also be reviewed. The new techniques that have been developed
5. To make microsensors and microactuators, such as bulk and surface silicon micromachining will be followed.
6. The fabrication process will include metal thin film e-beam evaporation, dielectric thin film growing using oxidation tube furnace, electrochemical deposition, and various kinds of chemical processes.

B. Learning Outcomes:

Upon Completion of the topics:

1. Be able to extend the principles of microfabrication to the development of micromechanical devices and the design of microsystems
2. Apply the principles of energy transduction, sensing and actuation on a microscopic scale.
3. Appreciate the effects of scaling, and the similarities and differences between Micromechanical assemblies and macroscopic machines.
4. Be able to analyse and model the behaviour of microelectromechanical devices and systems

C. Subject Matter:

UNIT – I

Overview of MEMS and Microsystems: Introduction to MEMS and Microsystems, Evolution of microsensors, MEMS, microfabrication, microelectronics and Microsystems. Typical MEMS and Microsystems products. Applications of MEMS. Introduction to smart materials and systems. (8)

UNIT – II

Working Principles of MEMS and Microsystems: Introduction to Microsensors and Microactuators. Electrical and mechanical concepts in MEMS. Sensing techniques for MEMS: Piezoresistive, Piezoelectric, Capacitive and Optical sensing methods. Piezoresistive sensor materials, piezoelectric materials. Applications for tactile, flow, inertia and pressure sensors. Microactuation techniques for MEMS: Actuation methods using thermal forces, piezoelectric crystals and electrostatic forces, Examples of MEMS based Microsensors and Microactuators. (12)

UNIT – III



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Materials and Fabrication Processes for MEMS and Microsystems Materials: Substrates and wafers, active substrate materials, Silicon as a substrate material, Silicon compounds, Gallium Arsenide, Quartz, piezoelectric crystals, packaging materials. Fabrication processes: Silicon Wafer Processing, Thin Film Deposition, Photolithography, Wet Etching and Dry Etching, Anisotropic Wet Etching and Isotropic Wet Etching, Plasma Etching, Diffusion, Ion Implantation, Oxidation, Chemical Vapor Deposition, Physical Vapor Deposition – Sputtering, Deposition by Epitaxy, Dry and Wet Etching Techniques, Micromachining processes: Bulk Micromachining and Surface Micromachining, the LIGA Process, other moulding techniques. Introduction to soft lithography and thick film processing. Overview of polymers in MEMS. MEMS for RF Applications. (14)

UNIT – IV

Electronic circuits for MEMS and Microsystems Semiconductor devices: Interface Electronics for MEMS. Overview of Diodes, BJT, MOSFET, CMOS, Electronic Amplifiers, Operational amplifiers, Differential amplifiers, Wheatstone Bridge circuits for measurement of resistance and analog to digital converters for MEMS and microsystems. Signal conditioning for Microsystems devices. Differential charge measurement, switched capacitor circuits for capacitance measurement. Control and Microsystems. Smart sensors and MEMS. MEMS Simulators. (12)

D. Teaching/Learning/Practice Pattern:

Teaching: 70%

Learning: 30%

E. Examination Pattern:

Theoretical Examination: Open book/ Regular examination and on line test.

F. READING LIST:

Text Books:

1. T. R. Hsu, "MEMS and Microsystems Design and Manufacture," Tata McGraw-Hill, 2002.
2. S. D. Sentaria, "Microsystem Design," Springer, 2004.
3. M. Madou, "Fundamentals of Microfabrication: The Science of Miniaturization," CRC Press, 2002.

Reference Books:

1. C. Liu, "Foundation of MEMS," Pearson, 2006.
2. N. Maluf, "An Introduction to Microelectromechanical System Design," Artech House, 2000.
3. J. W. Gardner, "Micro sensors: Principles and Applications," Wiley, 1994.

Magazines:

- 1.

Journals:

1. Journal of Micro/Nanolithography, MEMS, and MOEMS
2. Journal of Microelectromechanical Systems



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: Low Power VLSI Design

Module Code: ECE 942

Semester: 2nd

Credit Value: 3 [L=3, T=0, L=0]

Module Leader:

No. of Lectures:

A. Objectives:

The course is designed to meet with the objectives of

1. Identify sources of power in an IC.
2. Identify the power reduction techniques based on technology independent and technology dependent
3. Power dissipation mechanism in various MOS logic style.
4. Identify suitable techniques to reduce the power dissipation.
5. Design memory circuits with low power dissipation.

B. Learning Outcomes:

Upon Completion of the topics:

1. The student will get to know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays major role.
2. The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

C. Subject Matter:

UNIT – I

Review of CMOS circuits: MOS Transistor structure and device model, The CMOS inverter and other gates; why CMOS for Low Power? (3)

Power dissipation mechanisms: Static power – diode leakage, sub-threshold leakage; Dynamic power dissipation – short circuit power, switching power; Concept of signal activity, signal probability and activity, estimation of probability and activity in complex logic circuits; comparison of static and dynamic dissipation in CMOS circuits. (7)

UNIT – II

Sources of Static Dissipation: Charge leakage mechanisms in MOS transistors, Technology scaling and its effect; Threshold voltage (V_t) roll-off and its effect on sub-threshold current, Gate leakage – limitations of SiO₂ as gate oxide, high-k dielectric and its advantages. (6)

Managing Static Dissipation: Power supply gating, principles and circuit arrangements; Multiple threshold circuits, speed versus dissipation, strained Silicon MOS, technology requirements. (6)

UNIT – III

Dynamic dissipation management –Supply voltage scaling approaches: Static Voltage Scaling; Single-level Voltage Scaling (SVS), Speed vs dissipation, Speed management approaches, circuit level – Transistor sizing, Architecture level – Parallel and pipeline architectures, Algorithm level – Transformations to exploit concurrency, Static Voltage Scaling Design Procedure, Critical path and its management; Multi-level Voltage Scaling (MVS); Dynamic Voltage Scaling; Dynamic Voltage and Frequency Scaling (DVFS), DVFS architecture. (8)



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

UNIT – IV

Dynamic dissipation management – Switched capacitance minimization approaches: What is switched capacitor? Switched capacitor minimization techniques – Hardware/Software trade-off, Bus Encoding, Use of Number system, Glitching Power minimization, Architecture Level Optimization, Clock gating, State Encoding of FSM's. (8)

D. Teaching/Learning/Practice Practice Pattern:

Teaching: 70%

Learning: 30%

E. Examination Pattern:

Theoretical Examination: Open book/ Regular examination and on line test.

F. READING LIST:

Text Books:

1. Ajit Pal, Low Power VLSI Circuits and Systems, Springer 2015
2. K. Roy and S. Prasad, Low-Power CMOS VLSI Circuit Design, New York, Wiley-Interscience, 2000

Reference Books:

1. A. Chandrakasan and R. Brodersen, Low-Power CMOS Design, New York/Boston, IEEE Press/Springer, 1998/1995.

Magazines:

- 1.

Journals:

1. IEEE Transactions on Circuits and Systems I: Regular Papers



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: *RF IC Design*

Module Code: *ECE 943*

Semester: *2nd*

Credit Value: *3 [L=3, T=0, L=0]*

Module Leader:

No. of Lectures:

A. Objectives:

The course is designed to meet with the objectives of

1. The CMOS RF Front End (RFE) is a very crucial building block and in all of wireless and many high frequency wire-line systems. The RFE has few important building blocks within it including the Low Noise Amplifiers, Phase Locked Loop Synthesizers, Mixers, Power Amplifiers, and impedance matching circuits.
2. The present course will introduce the principles of operation and design principles associated with these important blocks.
3. The course will also provide and highlight the appropriate digital communication related design objectives and constraints associated with the RFEs

B. Learning Outcomes:

Upon Completion of the topics:

1. The student after completing this course must be able to translate the top level wireless communications system specifications into block level specifications of the RFE.
2. The student should be also able to carry out transistor level design of the entire RFE.

C. Subject Matter:

UNIT – I

Introduction: Basics of RF systems (1)

Review of Circuit theory: impedance concept, reflection and maximum power transfer. (2)

Tuned Circuits: Series and parallel RLC Networks, Q-factor, matching (3)

RF IC components: Resistance, capacitance and inductance, skin effect; Review of MOS Transistor. (4)

UNIT – II

Transmission Lines: The wave equation and its solutions, reflections, lossy transmission lines; Smith Chart and its use. (3)

RF Amplifiers: Amplifier topologies, bandwidth estimation, rise-time, delay and bandwidth, Shunt-series amplifiers, Cascaded amplifiers. (5)

Power amplifiers: Class A, B, AB and C amplifiers, Switching power amplifiers, RF Power amplifier design examples. (4)

UNIT – III

Noise: Signal and noise; Noise sources – thermal noise, flicker noise; noise figure, Intrinsic MOS Noise parameters, Power match vs noise match, Low noise amplifier concept. (5)

Oscillators: Oscillator topologies, Ring Oscillator, RF Resonators, Negative resistance oscillators (3)

UNIT – IV



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- Mixers:** Multiplier based mixers, large signal performance, Design examples. (3)
- Phase Locked Loops:** Linearized PLL Models; Phase detectors, charge pumps, loop filters; CMOS VCO, PLL Design examples (3)
- Frequency Synthesis:** Frequency dividers and multipliers, Frequency synthesizer examples (3)
- Radio architectures:** GSM, CDMA and UMTS system architectures. (2)

D. Teaching/Learning/Practice Practice Pattern:

Teaching: 70%

Learning: 30%

E. Examination Pattern:

Theoretical Examination: Open book/ Regular examination and on line test.

F. READING LIST:

Text Books:

1. The Design of CMOS Radio Frequency Integrated Circuits; Thomas H. Lee, Cambridge University Press (2004)
2. RF Microelectronics; Behzad Razavi, Prentice Hall (1997).

Magazines:

- 1.

Journals:

1. RFIC Virtual Journal, IEEE
2. Analog Integrated Circuits and Signal Processing



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: Memory Subsystem Design

Module Code: ECE 944

Semester: 2nd

Credit Value: 3 [L=3, T=0, L=0]

Module Leader:

No. of Lectures:

A. Objectives:

The course is designed to meet with the objectives of

1. To understand how a semiconductor memory works
2. Application of SRAM, DRAM & RRAM in industry
3. To study testing and fault modeling of different types of memory

B. Learning Outcomes:

Upon Completion of the topics:

1. Solve problems occurs in different industry graded memories.
2. Solve application specific memory testing
3. Discuss the high density memory packaging.
4. Students will be substantially prepared to take up prospective research assignments.

C. Subject Matter:

UNIT – I

Introduction: Combinational vs Sequential circuits, Concept of data storage; Types of memory – main and auxiliary memories, Random access vs. sequential access memories, Static vs Dynamic memories. (3)

Latches and Flip-flops: S-R, J-K and D flip-flops, Timing parameters of storage elements, CMOS implementation of latches and flip-flops. (7)

UNIT – II

Static RAM: Cell design – CMOS NAND and NOR memory cells, Read/Write operation, SRAM Cell layout, Address Decoders – Row and column decoders, Sense amplifiers. (5)

Memory array organization: Memory address and address decoders, row and column decoders, access time management, sense amplifiers. Single and multiport memories. (5)

UNIT – III

Dynamic RAM: Three-transistor cell, one-transistor cell, external characteristics of dynamic RAM (4)

Read-only Memories (ROM): Review of basic MOS physics – Threshold voltage and its control, EPROM, EEPROM, Flash memory, FRAM's; MOS ROM Cell arrays. (6)

UNIT – IV

Conditional Access Memory: CACHE, Memory management (4)

Advanced Topics: Magnetic memory cells - Giant Magneto-resistance phenomenon, spintronics. (4)

D. Teaching/Learning/Practice Practice Pattern:

Teaching: 70%

Learning: 30%



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E. Examination Pattern:

Theoretical Examination: Open book/ Regular examination and on line test.

F. READING LIST:

Text Books:

1. J.M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits- A Design Perspective, 2nd ed., PHI, 2003
2. Adel Sedra, Kenneth C. Smith, Microelectronic Circuits, The Oxford Series in Electrical and Computer Engineering

Reference Books:

1. R. Jacob Baker, Harry W. Li, David E. Boyce, CMOS: Circuit Design, Layout, and Simulation, IEEE Press Series on Microelectronic Systems

Magazines:

1. Electronics and Power Magazines.
2. Electron Devices magazines.

Journals:

1. IBM Journal of Research and Development.
2. IEEE Transactions of Semiconductor Manufacturing.
3. IEEE Transactions on Magnetics.



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: *Advanced Digital Signal Processing*

Module Code: *ECE 945*

Semester: *2nd*

Credit Value: *3 [L=3, T=0, L=0]*

Module Leader:

No. of Lectures:

A. Objectives:

The course is designed to meet with the objectives of

1. To introduce the basics of random signal processing
2. To learn the concept of estimation and prediction theory
3. To know about adaptive filtering and its applications
4. To understand the processing of speech signals

B. Learning Outcomes:

Upon Completion of the topics:

1. Estimate the spectra from finite duration signal
2. Analyze non-parametric methods and parametric methods for spectral estimation
3. Design different MMSE filters
4. Obtain models for prediction and Estimation
5. Design adaptive filters for different applications
6. Analyze different speech signal processing techniques
7. Represent acoustic signal in Short-term Fourier Transform

C. Subject Matter:

UNIT – I

Analog signal processing versus digital signal processing. Concepts of sampling, sampling theorem and aliasing. Introduction to Z-transform and its properties. Introduction to random signals and its properties. Correlation and its properties. Linear and circular convolution and their properties. (05)

Discrete Fourier transform (DFT) and inverse discrete Fourier transform (IDFT). Properties of DFT. Fast Fourier transform (FFT). Radix-2 decimation-in-frequency and decimation-in-time FFT algorithm. (06)

UNIT – II

Introduction to recursive and non-recursive systems. FIR and IIR systems. Design of Butterworth and Chebyshev analog filters. Discrete-time IIR filters from analog filters. Design of IIR filters using impulse invariant transformation, bilinear transformation, matched z-transformation etc (05)

FIR digital filters. Distortion less transmission of signal through a filter. Concepts of phase delay and group delay. Linear phase FIR filters and their properties. Design of digital filters by Fourier series method. Effect of truncation of impulse response. Filter design using windowing techniques. Gibbs phenomenon. Concepts of common window functions e.g. Hamming, Hann, Blackman etc. Design of FIR filters using frequency sampling techniques. Finite word length effects in digital filters. (06)

UNIT – III



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Representation of DSP algorithms; Iteration Bound: Definition, Examples, Algorithms for computing Iteration bound; Pipelining and Parallel Processing: Definitions, Pipelining and parallel processing of FIR filters. CORDIC based Implementations: Architecture, Implementation of FIR filter and FFT algorithm; Bit-Level arithmetic architectures: Parallel multipliers, Bit-serial multipliers, Bit-Serial FIR filter design and Implementation; Redundant arithmetic: Redundant number representation, Carry-free radix-2 addition and subtraction, radix-2 hybrid redundant multiplication architectures. (10)

UNIT – IV

Introduction to optimal and adaptive filters: Wiener filtering technique, adaptive filters and their applications. Introduction to multirate digital signal processing: decimation, interpolation, design of practical sampling rate converters. Applications.

Introduction to digital signal processors: Von Neumann architecture, Harvard architecture, modified Harvard architecture. (08)

D. Teaching/Learning/Practice Practice Pattern:

Teaching: 70%

Learning: 30%

E. Examination Pattern:

Theoretical Examination: Open book/ Regular examination and on line test.

F. READING LIST:

Text Books:

1. J. G. Proakis and M. G. Manolakis, "Digital Signal Processing: Principles, Algorithms and Applications," Pearson, 2006.
2. Oppenheim, Schaffer & Buck, "Discrete time Signal Processing," Prentice Hall, 1989.
3. U. Meyer-Baese, "DSP with FPGA," Springer, 2004.

Reference Books:

1. J. R. Jhonson, "Digital Signal Processing," Prentice Hall International, 1989.
2. K. K. Parhi, VLSI DSP Systems, Wiley, 2003.
3. B. P. Lathi, "Signal Processing & Linear System," Berkeley, Cambridge Press, 1998.
4. R.G. Lyons, "Understanding Digital Signal Processing," Pearson Education, 2004.
5. S. K. Mitra, "Digital Signal Processing," Tata McGraw-Hill,

Magazines:

1. IEEE Signal Processing Magazine

Journals:

1. Digital Signal Processing
2. IEEE Transactions on Signal Processing
3. IEEE Journal on Selected Topics in Signal Processing



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: Testing and Verification

Module Code: ECE 946

Semester: 2nd

Credit Value: 3 [L=3, T=0, L=0]

Module Leader:

No. of Lectures:

A. Objectives:

The course is designed to meet with the objectives of

1. In the VLSI design industry, a significant portion of work force and resources are been deployed in the test and validation of VLSI designs. The complexity of multimillion transistor based VLSI design calls for special techniques for efficiently testing and validating the VLSI design across all possible input, supply, speed and process corners. This has given rise to systematic areas of study in the form of design for test, automatic test pattern generation, fault diagnosis and these have all become very important areas from both research as well as routine industrial practice point of view.
2. The present course will introduce the student to the mathematical and scientific principles based on which systematic test and validation can be carried out on multimillion transistor VLSI design.

B. Learning Outcomes:

Upon Completion of the topics:

1. The student who completes this course will be familiar with the principles used in the construction VLSI Design For Test (DFT) tools.
2. The student will be able to adapt these to his specific industrial needs, also contribute to the development of more efficient tools from the fault coverage and speed point of view.

C. Subject Matter:

UNIT – I

Introduction: Purposes of testing, Difference between verification and Testing, Faults Errors and Failures, Test quality metrics, Testing Principle, Importance of Testing in new VLSI design flow. (3)

Fault Modeling: Fault models, Fault models at different abstraction levels, stuck-at-fault models, stuck-on and stuck-open fault models, geometric fault models, delay fault models, fault collapsing, fault equivalence and dominance. (5)

UNIT – II

Logic and fault simulation: Simulation for design verification, true-value simulation, compiled-code simulation, event-driven simulation, fault simulation algorithms and its utility. (4)

Combinational ATPG: ATPG principle, ATPG algebra, path sensitization method, D-frontiers and J-frontiers, D-algorithm, PODEM. (5)

UNIT – III

Sequential Circuit Testing: Basic concepts of sequential ATPG, differences with combinational ATPG, Time frame expansion, 9-valued ATPG algebra. (5)

Verification: Logic level and RTL level. (5)



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

UNIT – IV

Design for Testability: Controllability and observability, Ad-hoc testing, scan-based testing, boundary scan, level sensitive scan design, BIST architecture and techniques. (10)

D. Teaching/Learning/Practice Pattern:

Teaching: 70%

Learning: 30%

E. Examination Pattern:

Theoretical Examination: Open book/ Regular examination and on line test.

F. READING LIST:

Text Books:

1. Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing, for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers (2000).
2. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, "Digital Systems Testing and Testable Design," Revised, IEEE Press (1990).
3. Samiha Mourad and Yervant Zorian, "Principles of Testing Electronic Systems", Wiley (2000).

Magazines:

- 1.

Journals:

1. Journal of Electronic Testing
2. IEEE Design & Test



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: *Microelectronics Technology Laboratory*

Module Code: *ECE 972*

Semester: *3rd*

Credit Value: *4 [L=0, T=0, P=8]*

Module Leader:

No. of Lectures:

A. Objectives:

The course is design to meet with the objectives of:

1.

B. Learning outcomes:

Upon completion of the subjects:

1.

C. Subject Matter:

1. Mask Design and Photolithography
2. Metallization and measurement of contact resistance
3. Silicon oxidation and measurement of oxide thickness
4. Fabrication of MOS capacitor and its characterization
5. Dopant Diffusion and resistivity measurement
6. Fabrication and characterization of simple devices
7. Hall measurement*

* Optional: subject to available facility.

Set-up required:

1. Metallization Unit
2. Oxidation and diffusion (p-dopant only) Unit comprising
 - a. Furnaces for Oxidation and Diffusion (up to 1100o C) – Two units
 - b. Gas plumbing for furnaces with flow control and scrubber at exhaust
3. Simple photolithographic set up comprising
 - a. Yellow room
 - b. Photoresist spinner
 - c. UV lamp and contact printing frame
4. Deionized water plant
5. Optical microscope
6. I – V and C – V measurement instruments
7. Magnet for Hall Measurement*



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SYLLABUS FOR M-TECH. (VLSI DESIGN & EMBEDDED SYSTEM)

Name of the Module: Mini Project

Module Code: ECE 973

Semester: 3rd

Credit Value: 4 [L=0, T=0, P=8]

Module Leader:

No. of Lectures:

Mini – Project (Suggested):

Students may be given a course project to do in the group of four students. This will be evaluated through demo and viva. This mini project should have strong embedded system component.